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Conc'd.*

a translation control circuit coupled to the address translator to program the entries in the address translator;

wherein the address translator is to translate an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface.

31. (previously added) The apparatus of claim 30, wherein:

the address translator is further to translate an address on the second interface into a second address on the first interface having a greater number of bits than the address on the second interface.

32. (previously added) The apparatus of claim 30, wherein:

the address translator comprises a graphics translation lookaside buffer.

REMARKS

Claims 8-9, 12-14, 23-29 and 30-32 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent no. 6,477,623 ("Jeddeloh") in view of U.S. patent no. 5,802,605 ("Alpert").

Claims 19-21 have been rejected under 35 USC 103(a) as being unpatentable over Jeddeloh in view of U.S. patent no. 5,574,877 ("Dixit").

Claim 22 has been rejected under 35 USC 103(a) as being unpatentable over Jeddeloh and Dixit in view of Alpert.

Claims 15-18 and 23-28 have been rejected under 35 USC 103(a) as being unpatentable over Jeddeloh, Alpert, and Dixit.

Applicants respectfully traverse these rejections in view of the amendment because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

* Independent claims 8, 15, 19, and 30 each recite that an address from a bus controller is translated into a translated address having more bits than the address from the bus controller. The Office action admits that Jeddeloh does not teach this limitation, and relies on Alpert to provide it. However, Alpert never mentions translating addresses from bus controllers, and does not discuss translation of addresses from any device other than a processor. It would not be obvious to extend the address translator of Alpert from a processor to a bus controller. Processors are typically highly integrated with memory, with a constant need to access all areas of physical memory. Bus controllers, on the other hand, generally perform only sporadic access to memory, and may not be able to justify the cost of a translator that would enable such universal memory access.

The remaining claims depend from claims 8, 15, 19 and 30, and therefore contain the same limitations not disclosed or suggested by the cited references.

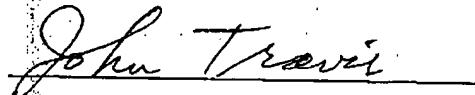
CONCLUSION

For the foregoing reasons, Applicant submits that the application is now in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. If any fee deficiency or overpayment is found in connection with this application, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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